1. What is claimed:A metal-oxide-compound semiconductor field effect transistor comprising:

a nitride compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first and second layer;

said first layer substantially comprising compounds of gallium and oxygen

said second layer comprising compounds of gallium and oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure,

source and drain regions self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on said source and drain areas;

wherein gate electrode comprises a metal selected from the group refractory gate metals and combinations thereof;

wherein the complete nitride MOS structure is built upon a a sapphire, silicon, SOI, AlN, or GaN substrate.

2. The transistor of claim 1 wherein said first layer forms an atomically abrupt interface with said upper surface.
3. The transistor of claim 1 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of indium oxygen, gallium oxygen and at least one rare-earth element.
4. The transistor of claim 3 wherein said gate insulator structure further comprises a third layer containing oxygen and a rare earth elements that do not include indium or gallium.
5. The transistor of claim 1 wherein said field effect transistor is an enhancement mode transistor.
6. The transistor of claim 1 wherein said field effect transistor is a depletion mode transistor.
7. The transistor of claim 1 wherein said first layer has a thickness of more than 3 angstroms and less than 25 angstroms.
8. The transistor of claim 1 wherein said gate insulator structure has a thickness of 10-300 angstroms.

9. The transistor of claim 1 wherein said first layer forms an interface with said upper surface that extends less than two atomic layers in depth of structural interface modulation.

10. The transistor of claim 1 wherein said first layer and said gate insulator structure protects said upper surface.

11. The transistor of claim 1 wherein said gate electrode comprises a refractory metal which is stable in the presence of the top layer of the gate insulator structure at above 700°C.

12. The transistor of claim 1 wherein said source and drain regions are regrown using a doped nitride based semiconductor to provide for one of an n-type and/or one p-type region.

13. The transistor of claim 1 wherein said source and drain regions provide one of an n-channel or p-channel.

14. The transistor of claim 1 wherein source and drain implants comprise at least one of Be, Si, Te, Sn, C, and Mg.

15. The transistor of claim 1 wherein said upper surface comprises GaN.

16. The transistor of claim 1 wherein said upper surface comprises $In_xGa_{1-x}N$.

17. The transistor of claim 1 wherein said upper surface comprises $Al_xGa_{1-x}N$.

18. The transistor of claim 1 wherein said upper surface comprises AlN.

19. A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure on said upper surface, said gate insulator structure comprising a first layer, a second layer, and a third layer;

said first layer substantially comprising compounds of indium and oxygen

said second layer comprising compounds of indium gallium and oxygen and at least one rare earth element;

said third layer above said second layer, said third layer substantially comprising gallium oxygen and at least one rare earth element, said third layer being insulating;

a gate electrode positioned on said gate insulator structure;

source and drain regions self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on source and drain areas;

wherein gate electrode comprises a metal selected from the group of refractory metals and combinations thereof.

20. The transistor of claim 22 wherein said first layer forms an atomically abrupt interface with said upper surface.

21. The transistor of claim 22 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of indium, gallium, oxygen and at least one rare-earth element.

22. The transistor of claim 22 wherein said gate insulator structure further comprises a third layer containing indium, gallium, and oxygen.

23. The transistor of claim 22 wherein said field effect transistor is an enhancement mode transistor.

24. The transistor of claim 22 wherein said field effect transistor is a depletion mode transistor.

25. The transistor of claim 22 wherein said first layer has a thickness of more than 3 angstroms and less than 25 angstroms.

26. The transistor of claim 22 wherein said gate insulator structure has a thickness of 10-300 angstroms.

27. The transistor of claim 22 wherein said first layer forms an interface with said upper surface that extends less than four atomic layers in depth of structural interface modulation.

28. The transistor of claim 22 wherein said first layer and said gate insulator structure protects said upper surface.

29. The transistor of claim 22 wherein said gate electrode comprises a refractory metal which is stable in the presence of the top layer of the gate insulator structure above 700°C.

30. The transistor of claim 22 wherein said source and drain regions are regrown using a epitaxial deposition technique to provide for n-type and p-type regions.

31. The transistor of claim 22 wherein said source and drain regions are ion implanted to provide for one of an n-type or p-type region.

32. The transistor of claim 22 wherein said source and drain regions provide one of an n-channel or p-channel.

33. The transistor of claim 22 wherein said source and drain implants comprise at least one of Be, Si, Te, Sn, C, and Mg.

34. The transistor of claim 22 wherein said upper surface comprises GaN.

35. The transistor of claim 22 wherein said upper surface comprises $In_xGa_{1-x}N$.

36. The transistor of claim 22 wherein said upper surface comprises $Al_xGa_{1-x}N$.

37. A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprise indium, gallium, oxyen, and at least one rare earth element.

a gate electrode positioned on said gate insulator structure;

source and drain regions self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein gate electrode comprises a metal selected from the group of refractory metals and combinations thereof.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising;

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain self-aligned to the gate electrode; and source and drain ohmic contacts positioned on source and drain areas, wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}N$; and wherein said transistor is integrated together with similar or complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit

39. A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first and second layer; said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen

said second layer comprising compounds of oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure.

40. A structure of claim 39 wherein said gate electrode comprises a refractory metal.

41. A structure of claim 41 wherein said gate electrode comprises a member of the group Pt, Ir, W, WN, Mo, Ru, TiWN, WSi, and combinations thereof.

42. A structure of claim 39 wherein said gate insulator structure further comprises a third layer.

43. A structure of claim 39 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

44. A structure of claim 39 wherein a composition of said third layer varies monotonically with depth in said third layer.

45. The structure of claim 39 wherein said gate insulator structure further comprises a fourth layer.

46. The structure of claim 39 wherein compounds of said fourth layer comprising gallium and oxygen.

47. A structure of claim 39 wherein compounds of said fourth layer comprising gallium and oxygen and further comprising a rare earth element.

48. A structure of claim 39 wherein compounds of said fourth layer comprising gallium oxygen and one rare earth and further comprising indium.

49. The structure of claim 39 wherein said first layer is adjacent and in contact with said upper surface.

50. The structure of claim 39 wherein said source and drain contacts are ion implanted.

51. The structure of claim 39 wherein said source and drain contacts are annealed in an ultra high vacuum environment.

52. The structure of claim 39 wherein said gate insulator structure passivates said upper surface.

53. A method for forming a metal-oxide-compound semiconductor field effect transistor, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of indium, gallium, and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and depositing a gate electrode positioned on said gate insulator structure.

54. The method of claim 53 comprising rapid thermal annealing said structure in a UHV environment.

55. The method of claim 53 wherein said rapid thermal annealing comprising annealing between 700 and 1350 degrees Centigrade.

56. The transistor of claim 33 wherein said first layer forms an atomically abrupt interface with said upper surface.

57. The transistor of claim 53 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of indium, gallium, oxygen and at least one rare-earth element.

58. The transistor of claim 53 wherein said field effect transistor is an enhancement mode transistor.

59. The transistor of claim 53 wherein said field effect transistor is a depletion mode transistor.

60. The transistor of claim 53 wherein said first layer has a thickness of more than 3 angstroms and less than 25 angstroms.

61. The transistor of claim 53 wherein said gate insulator structure has a thickness of 10-300 angstroms.

62. The transistor of claim 53 wherein said first layer forms an interface with said upper surface that extends less than four atomic layers in depth of structural interface modulation.

63. The transistor of claim 53 wherein said first layer and said gate insulator structure protects said upper surface.

64. The transistor of claim 53 wherein said gate electrode comprises a refractory metal which is stable in the presence of the top layer of the gate insulator structure above 700°C.

65. The transistor of claim 53 wherein said source and drain regions are regrown to provide for transistor ohmic contacts separated into n-type or p-type regions.

66. The transistor of claim 53 wherein said source and drain regions provide one of an n-channel or p-channel.

67. The transistor of claim 53 wherein said source and drain implants comprise at least one of Be, Si, Te, Sn, C, and Mg.

68. The transistor of claim 63 wherein said upper surface comprises GaN.

69. The transistor of claim 63 wherein said upper surface comprises $In_xGa_{1-x}N$.

70. The transistor of claim 63 wherein said upper surface comprises $Al_xGa_{1-x}N$.

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